CLAIMS:

1. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

providing a series of spaced trenches at least 2000 Angstroms deep within the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates; and

implanting conductivity enhancing impurity into the semiconductor substrate beneath the trenches, along sidewalls of the trenches and between the trenches and forming therefrom a continuous line of source active area within the semiconductor substrate along at least a portion of the line of floating gates.

2. The method of claim 1 wherein the spaced trenches are provided by etching trenches into the semiconductor substrate and subsequently filling the trenches by depositing insulating material, and thereafter removing a majority of said insulating material from the trenches immediately adjacent the line of floating gates along said continuous line of source active area being formed.

3. The method of claim 1 comprising providing the series of spaced trenches before forming the line of floating gates.

4. The method of claim 1 wherein the implanting comprises at least one implant conducted at an angle from normal to a general orientation of the semiconductor substrate.

5. The method of claim 1 wherein the spaced trenches have sidewalls, the sidewalls extending along a line from an outer surface of the semiconductor substrate to a floor of the respective trenches, the line being straight along a majority of its length.

6. The method of claim 1 wherein the spaced trenches are provided by LOCOS and removal of oxide produced by said LOCOS.

7. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

providing an alternating series of trench isolation regions and active area regions in the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates;

removing isolation material from trenches of the trench isolation regions;

after the removing, implanting conductivity enhancing impurity into the semiconductor substrate within the active area regions and beneath the trenches and forming therefrom a continuous line of source active area within the semiconductor substrate along at least a portion of the line of floating gates.

8. The method of claim 7 wherein the trench isolation regions are provided by etching trenches into the semiconductor substrate and subsequently filling the trenches by depositing insulating material.

9. The method of claim 7 comprising providing the series of spaced trenches before forming the line of floating gates.

10. The method of claim 7 wherein the implanting comprises at least one implant conducted at an angle from normal to a general orientation of the semiconductor substrate.

11. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

etching into the semiconductor substrate to form a series of spaced trenches within the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates; and

conducting at least one conductivity enhancing impurity implant into the semiconductor substrate at an angle away from normal to a general orientation of the semiconductor substrate to implant at least along sidewalls of the trenches and between the trenches, and forming a continuous line of source active area within the semiconductor substrate along at least a portion of the line of floating gates.

12. The method of claim 11 comprising conducting at least one conductivity enhancing impurity implant into the semiconductor substrate at an angle normal to the general orientation of the semiconductor substrate.

13. The method of claim 11 wherein the trenches are effectively deep to preclude forming a continuous implant region at bases of the trenches from said at least one angled implant, and further comprising conducting at least one conductivity enhancing impurity implant into the semiconductor substrate at an angle normal to the general orientation of the semiconductor substrate to implant into the trench bases.

14. The method of claim 11 comprising forming trenches to be at least 3000 Angstroms deep, and conducting at least one conductivity enhancing impurity implant into the semiconductor substrate at an angle normal to the general orientation of the semiconductor substrate.

15. The method of claim 11 wherein the conducting occurs after filling the spaced trenches by depositing insulating material and removing a majority of said insulating material from the trenches immediately adjacent the line of floating gates along said continuous line of source active area being formed.

16. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

etching into the semiconductor substrate to form a series of spaced trenches within the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates, the spaced trenches comprising sidewall portions angled at least 15° from normal to a general orientation of the semiconductor substrate;

depositing insulating material to within the trenches and thereafter removing a majority of said insulating material from the trenches immediately adjacent the line of floating gates along a continuous line of source active area being formed along at least a portion of the line of floating gates; and

implanting conductivity enhancing impurity into the semiconductor substrate beneath the trenches, along the trench sidewalls and between the trenches and forming therefrom said continuous line of source active area within the semiconductor substrate along at least a portion of the line of floating gates.

17. The method of claim 16 wherein the trench sidewall portions are angled at least 20° from normal to the general orientation of the semiconductor substrate.

18. The method of claim 16 wherein the trench sidewall portions are angled at least 30° from normal to the general orientation of the semiconductor substrate.

19. The method of claim 16 wherein the trench sidewall portions are angled at least 40° from normal to the general orientation of the semiconductor substrate.

20. The method of claim 16 wherein the implanting comprises at least one implant conducted at an angle away from normal to the general orientation of the semiconductor substrate.

21. The method of claim 16 wherein the implanting comprises at least one implant conducted at an angle normal to the general orientation of the semiconductor substrate.

22. The method of claim 16 wherein the implanting comprises at least one implant conducted at an angle normal to the general orientation of the semiconductor substrate, and at least one implant conducted at an angle away from normal to the general orientation of the semiconductor substrate.

23. The method of claim 16 comprising etching the series of spaced trenches before forming the line of floating gates.

24. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

providing an alternating series of trench isolation regions and active area regions in the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates, the series of active areas defining discrete transistor source areas separated by trench isolation regions;

forming a conductive line over the discrete transistor source areas and trench isolation regions separating same adjacent and along at least a portion of the line of floating gates, the conductive line electrically interconnecting said discrete transistor source areas; and

providing source forming conductivity enhancing impurity into the discrete transistor source areas.

25. The method of claim 24 wherein a majority of the source forming impurity is provided before forming the conductive line.

26. The method of claim 24 wherein a majority of the source forming impurity is provided commensurate with or after forming the conductive line.

27. The method of claim 24 comprising providing the series of trench isolation regions before forming the line of floating gates.

28. The method of claim 24 wherein the conductive line comprises conductively doped polysilicon capped with a conductive silicide layer.

29. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate;

providing an alternating series of trench isolation regions and active area regions in the semiconductor substrate in a line adjacent and along at least a portion of the line of floating gates, the series of active areas defining discrete transistor source areas separated by trench isolation regions;

forming conductively doped semiconductor material over the discrete transistor source areas and trench isolation regions separating same adjacent and along at least a portion of the line of floating gates which electrically interconnects said discrete transistor source areas;

out diffusing source forming conductivity enhancing impurity into the discrete transistor source areas from the conductively doped semiconductor material; and

patterning the conductively doped semiconductor material into a conductive line.

30. The method of claim 29 wherein the conductively doped semiconductor material is capped with a conductive silicide layer.

31. The method of claim 29 wherein the conductively doped semiconductor material is capped with a conductive silicide layer prior to the patterning.

32. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side;

depositing an insulative sidewall forming layer over the line of floating gates; and

forming an insulative sidewall spacer on one of the source side and the drain side before the other by anisotropically etching the insulative sidewall forming layer.

33. The method of claim 32 wherein the source side insulative spacer is formed before the drain side insulative spacer.

34. The method of claim 32 wherein the drain side insulative spacer is formed before the source side insulative spacer.

35. The method of claim 32 wherein the other side is masked with photoresist while the insulative sidewall spacer on the one side is being formed.

36. A method of forming a line of FLASH memory cells comprising:

forming a line of floating gates over a semiconductor substrate, the line of floating gates having a source side and a drain side;

depositing an insulative sidewall forming layer over the line of floating gates; and

in one anisotropic etching step of the insulative sidewall forming layer, forming an insulative sidewall spacer on only one of the source side and the drain side and not the other.

37. The method of claim 36 further comprising in another anisotropic etching step, forming an insulative sidewall spacer on the other side.

38. The method of claim 36 wherein the other side is masked with photoresist while the insulative sidewall spacer on the one side is being formed.

39. The method of claim 36 wherein no insulative sidewall spacer is ever formed on the other side.

40. The method of claim 36 wherein the one side is the source side.

41. The method of claim 36 wherein the one side is the drain side.

42. A line of FLASH memory cells comprising:

a line of floating gates received over a semiconductor substrate;

an alternating series of trench isolation regions and active area source regions in the semiconductor substrate formed in a line along at least a portion of the line of floating gates, the source regions being conductively doped with a conductivity enhancing impurity and separated by the trench isolation regions; and

a conductive line formed over the source regions and trench isolation regions along at least a portion of the line of floating gates, the conductive line electrically interconnecting said source regions.

43. The line of claim 42 wherein the trenches are formed at least 2000 Angstroms deep into the semiconductor substrate.

44. The line of claim 42 wherein the conductive line comprises conductively doped polysilicon capped with a conductive silicide.